What Is Claimed Is:

1. A method to form a gate in a semiconductor device comprising:

forming a gate insulation film on a semiconductor substrate;

forming a gate polysilicon layer on the gate insulation film;

performing a first dry etching process on the gate polysilicon layer under first process conditions, wherein upper sidewall polymers are formed on an upper portion of the gate polysilicon layer;

performing a second dry etching process on the gate polysilicon layer under second process conditions, wherein lower sidewall polymers are formed on sidewalls of a lower portion of the gate polysilicon layer by sidewall polymerization, the lower sidewall polymers being thinner than the upper sidewall polymers; and

performing a third dry etching process on the gate polysilicon layer to remove the upper and lower sidewall polymers, wherein the lower portion of the gate polysilicon layer is over etched so that a CD of the upper portion of the gate is greater than a CD of the lower portion of the gate.

2. A method as defined in claim 1, wherein at least one of the first dry etching process and the second dry etching process is performed in multi-stages so that the gate has a sidewall profile has a multi-layered structure wherein a CD of each layer is decreased relative to an immediately preceding layer.

3. A method as defined in claim 1, wherein the CD of the lower portion of the gate is set by controlling an over etching time period of the third dry etching process.

4. A method as defined in claim 1, wherein the first process conditions are set such that CF_4, HBr, Cl_2 and HeO_2 are used as the first etching gases; feed rates of the CF_4, HBr, Cl_2 and HeO_2 are about 1 ~ 100 sccm, about 5 ~ 180 sccm, about 1 ~ 100 sccm and about 1 ~ 50 sccm, respectively; a source power and a bias power of a plasma range from about 10 W to about 1000 W and from about 1 W to about 200 W, respectively; and a pressure of the plasma ranges from about 1 mT to about 30 mT.

5. A method as defined in claim 1, wherein the second process conditions are set such that HBr, Cl_2 and HeO_2 are used as the second etching gases; feed rates of the HBr, Cl_2 and HeO_2 are about 1 ~ 300 sccm, about 1 ~ 200 sccm and about 1 ~ 50 sccm, respectively; a source power and a bias power of a plasma range from about 10 W to about 500 W and from about 5 W to about 150 W, respectively; and a pressure of the plasma ranges from about 1 mT to about 50 mT.

6. A method as defined in claim 1, wherein the third dry etching is performed under third process conditions in which HBr, HeO_2 and O_2 are used as etching gases; feed rates of the HBr, HeO_2 and O_2 are about 1 ~ 300 sccm, about 1 ~ 100 sccm and about 0.1 ~ 50 sccm, respectively; a source power and

a bias power of a plasma range from about 10 W to about 2000 W and from about 1 W to about 300 W, respectively; and a pressure of the plasma ranges from about 1 mT to about 200 mT.